amendments, claims 16-33 (2 independent claims; 18 total claims) remain pending in the application. Reconsideration is respectfully requested.

As a preliminary matter, the undersigned thanks the Examiner for his time and consideration during the telephone interview of September 26, 2000. As stated during the September 26, 2000 interview, Applicants believe the pending claims are patentable over the cited references because none of the references, either alone or in any combination, discloses or teaches, *inter alia*, an interconnect structure having any of the following elements: a protective layer which "covers at least one vertical portion of a low-k material"; a protective layer which is "configured to provide etch selectivity between said protective layer and said second dielectric material"; or a "spacer".

Rejections Under 35 U.S.C. §112

Claims 30 and 31 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as their invention. In particular, the Examiner states that claims 30 and 31 are incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections. The Examiner further states that the omitted structural cooperative elements include the relationship between the liner and each of the following elements: the metal lines, the low-k dielectric, the protective layer, and the conductive feature. The Examiner contends that it is not known where the liner of claim 30 is disposed with respect to the rest of the claimed structure. Applicants respectfully traverse this rejection.

As amended, claims 30 and 31 recite that the liner is disposed within a feature formed within the second dielectric material. Accordingly, claims 30 and 31 particularly point out the essential structural cooperative relationships between the various elements recited in the claims, and Applicants respectfully request the withdrawal of the rejection of claims 30 and 31 under 35 U.S.C. §112, second paragraph.

Rejections Under 35 U.S.C. §102

Claims 16-20, 23, and 27-29 stand rejected under 35 U.S.C. §112(b) as being anticipated by Havemann *et al.*, U.S. Patent No. 5,747,880, issued May 5, 1998 (hereinafter "Havemann"). In particular, the Examiner states that, regarding claim 16, Havemann teaches an interconnect comprising: one or more metal lines (24) having gaps between them; low-k material (28) between the metal lines, wherein the low-k material has a height and one or more vertical portions; a protective layer (56) over the metal lines and the low-k material, wherein the protective layer covers a vertical portion of the low-k material; a dielectric layer (30) over the protective layer; a via in the dielectric layer; a metal (32) filling the via; a second metal layer (34) over the dielectric layer; and an opening in the protective layer to allow contact between the metal in the via and the metal lines. Regarding claim 17, the Examiner states that Havemann teaches an interconnect structure wherein the protective layer comprises an oxide. Regarding claim 18, the Examiner states that Havemann teaches an interconnect structure wherein the oxide comprises silicon dioxide (Col. 7, lines 3 and 4). Regarding claims 19 and 29, the Examiner states that Havemann teaches an interconnect wherein the protective layer comprises dielectric material. Regarding claims 20, 23, and 27, the Examiner states that Havemann teaches an interconnect wherein the low-k material comprises a porous silicon dioxide and the protective layer is silicon nitride. Regarding claim 28, the Examiner states that Havemann teaches an interconnect structure comprising a plurality of metal lines (24) on a substrate; low-k dielectric (28) between the metal lines; a second dielectric (30) above the metal lines; a protective layer (56) between the second dielectric and the low-k dielectric; and a conductive feature (32) within the second dielectric and the protective layer, wherein the conductive feature is in contact with at least one of the metal lines. Applicants respectfully traverse this rejection.

Havemann generally discloses structures for hybrid porous/non-porous dielectrics for use as semiconductor insulators. Specifically, Havemann discloses an interconnect structure comprising a substrate (22); a plurality of metal lines (24); a

porous dielectric material (28) configured to fill the gaps (28) between the metal lines; a conformal sublayer (56) disposed directly over the porous dielectric layer and the metal lines; and a planarized non-porous dielectric (30) applied over the conformal sublayer (Col. 7 line 55 – Col. 8, line 18; FIG. 6F). As disclosed in Havemann, conformal layer 56 is a dry-processed chemical vapor deposition (CVD) layer which avoids the use of solvents capable of wetting the pores in the porous layer (28) (Col. 8, lines 5-14). Non-porous dielectric layer (30) is then deposited using a spin-on glass technique to achieve a planarized, top dielectric sublayer (Col. 8, lines 14-18). Importantly, Havemann does not disclose a protective layer which covers at least one vertical portion of a low-k material. Moreover, Havemann does not disclose that the layers (56) and (30) comprise materials which are selected or configured to provide etch selectivity between the layers (56) and (30).

Applicants' independent claim 16 recites, *inter alia*, a protective layer which covers at least one vertical portion of a low-k material. The Examiner alleges that Havemann discloses a low-k material (28) having one or more vertical portions and a protective layer (56) which covers a vertical portion of the low-k material. However, Applicants assert that Havemann does not disclose a protective layer covering vertical portions of a low-k material. As seen in FIG. 6F of the Havemann reference, the low-k, porous dielectric (28) comprises a single horizontal surface that is level with the top of conductors (24). Conformal sublayer (56) is horizontally disposed over both the low-k material (28) and the conductors (24). The conformal sublayer (56) nowhere covers a vertical portion of the low-k material (28). While FIG. 6G shows the vertical sidewalls of the via (52), the conformal sublayer (56) is not disposed on the vertical sidewalls. Moreover, as illustrated, the sidewalls of the via (52) comprise the non-porous dielectric material (30), not the porous, low-k material (28). Thus, Havemann does not disclose a protective layer which covers at least one vertical portion of a low-k material.

For, *inter alia*, the above reasons, Applicants assert that the Havemann reference fails to disclose each and every element of Applicants' independent claim 16. Accordingly, claim 16 (and claims 17-27, each of which variously depend therefrom) is

not anticipated by the Havemann reference, and Applicants therefore respectfully request the withdrawal of the rejection of claims 16-20, 23, and 27 under 35 U.S.C. §102(b).

As amended, Applicants' independent claim 28 recites, *inter alia*, a protective layer configured to provide etch selectivity between the protective layer and the second dielectric material. Applicants assert that Havemann does not disclose this element. The Havemann reference discloses a conformal sublayer (56) deposited by CVD and formed above conductors (24) and porous dielectric (28). A non-porous dielectric layer (30) is then formed above the conformal sublayer and preferably is deposited by a spin-on glass (SOG) technique. As disclosed by Havemann, the conformal sublayer is deposited by a dry-processed CVD to avoid using solvents which would wet the porous dielectric layer (Col. 8, lines 9-14). The non-porous dielectric is applied as an SOG oxide to accomplish a planarized interlayer dielectric (Col. 8, lines 14-18). Thus, Havemann teaches the importance of differentially applying conformal sublayer (56) and non-porous dielectric (30) to protect the porous dielectric layer (28) while still achieving a planarized dielectric surface. However, nowhere does Havemann disclose that layers (56) and (30) preferably comprise distinct materials or materials that have distinct etch selectivities. In fact, the table at column 9 discloses that "preferred or specific examples" for "drawing elements" (30) and (56) both include silicon dioxide. Thus, Applicants assert that not only does Havemann not disclose or teach a protective layer configured to provide etch selectivity between the protective layer and the non-porous dielectric material, but Havemann specifically teaches away from having layers (30) and (56) necessarily comprising different materials, which therefore also teaches away from providing layers (30) and (56) with etch selectivity. Consequently, Applicants assert that Havemann does not disclose or teach a protective layer configured to provide etch selectivity between the protective layer and the second dielectric material.

For, *inter alia*, the above reasons, Applicants assert that Havemann fails to disclose each and every element of Applicants' independent claim 28. Accordingly, claim 28 (and claims 29-33, each of which variously depend therefrom) is not

anticipated by the Havemann reference, and Applicants therefore respectfully request the withdrawal of the rejection of claims 28 and 29 under 35 U.S.C. §102(b).

Rejections Under 35 U.S.C. §103

Allegedly Admitted Prior Art and Chiang

Claims 16-21 and 23-31 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over purportedly admitted prior art in view of Chiang *et al.*, U.S. Patent No. 5,886,410, issued on March 23, 1999 (hereinafter "Chiang"). More particularly, the Examiner states that while the purportedly admitted prior art does not teach a protective layer disposed on top of the low-k material, wherein the protective layer has openings for allowing the metal in the vias to contact the first metal lines, Chiang teaches an interconnect structure having a protection layer (110) disposed on top of the low-k material layer, wherein the protection layer has openings for allowing metal in the vias to contact the metal lines. The Examiner further states that it would have been obvious to one of ordinary skill at the time of the invention to incorporate Chiang with the allegedly admitted prior art since the protection layer would improve the mechanical strength of the interconnect system. In addition, the Examiner states that it is obvious to form openings in the protection layer in order to electrically connect the conductive lines.

In response to Applicants' arguments filed on March 14, 2000, the Examiner states Applicants' arguments as follows: (1) Chiang does not teach a protective layer; (2) the allegedly admitted prior art and Chiang teach the same invention; and (3) Chiang does not teach a protective layer over the metal lines and a vertical portion of the low-k material. The Examiner contends that the hardmask taught by Chiang will have protective properties. The Examiner further contends that the allegedly admitted prior art does not teach another dielectric layer above the oxide layer. Additionally, the Examiner alleges that, as seen in FIG. 6 and 7, the protective layer is formed over the metal line (106) and that the protective layer is over vertical portions of the low-k dielectric. The Examiner also contends that Applicants' arguments with respect to claim

22 are moot in view of the new ground(s) of rejection. Applicants respectfully traverse this rejection.

Chiang generally discloses an interconnect structure including a low-k dielectric feature formed between metal lines and a hard mask deposited onto the low-k material. Chiang further discloses depositing metal over the hard mask material to form a second level having additional metal lines. Significantly, Chiang does not disclose a protective layer which covers at least one vertical portion of a low-k material. Additionally, Chiang does not disclose a second dielectric material formed above the metal lines, nor does Chiang disclose a protective layer interposed between the low-k dielectric structures and the second dielectric material.

Applicants assert that, even if the proposed combination were made, Applicants' claimed invention would not be obtained. Specifically, neither the allegedly admitted prior art nor Chiang, either alone or in combination, discloses, teaches, or suggests all of the elements recited in Applicants' claims 16-21 and 23-31. In particular, with respect to independent claim 16, Applicants assert that Chiang does not disclose, teach, or suggest a protective layer which covers at least one vertical portion of a low-k material. As seen in any of FIGS. 1-7 of the Chiang reference, low-k material (108) forms a single horizontal surface across the interconnect system (100). Moreover, hard mask (110) is formed over the single horizontal surface of low-k material (108). Nowhere does Chiang disclose, teach, or suggest covering at least one vertical portion of a low-k material with a protective layer. Consequently, Applicants assert that neither the allegedly admitted prior art nor Chiang disclose, teach, or suggest all of the elements of Applicants' claimed invention.

Moreover, regarding independent claim 28, Applicants assert that neither the allegedly admitted prior art nor Chiang discloses, teaches, or suggests "a second dielectric material formed above said metal lines"; "a protective layer interposed between said low-k dielectric structures and said second dielectric material"; and "a conductive feature formed within said second dielectric material and said protective layer". As seen in FIG. 4 of the Chiang reference, for example, Chiang teaches the

formation of via holes (116) through a hard mask layer (110) and through a low-k material (108), where the hard mask layer (110) is formed directly over the low-k material (108). Even if, *arguendo*, the hard mask layer (110) could correspond to a protective layer, Chiang does not disclose a protective layer interposed between a low-k material and a second dielectric material. Furthermore, since Chiang does not disclose "a second dielectric material", Chiang also does not disclose a conductive feature formed within a second dielectric material and the protective layer. Accordingly, Applicants assert that the Chiang reference does not disclose, teach, or suggest all of the elements of Applicants' claimed invention.

For, *inter alia*, the above reasons, Applicants assert that independent claim 16 (and claims 17-27, which variously depend therefrom) and independent claim 28 (and claims 29-31, each of which depend variously therefrom) are not rendered obvious by the allegedly admitted prior art in view of Chiang. Accordingly, claims 16-21 and 23-31 are patentable over the allegedly admitted prior art and the reference cited by the Examiner, and Applicants therefore respectfully request the withdrawal of the rejection of claims 16-21 and 23-31 under 35 U.S.C. §103(a).

Allegedly Admitted Prior Art, Chiang, and Chen

Claims 22, 32, and 33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over allegedly admitted prior art and Chiang, as applied to claims 16-21 and 28, in view of Chen *et al.*, U.S. Patent No. 5,317,192, issued on May 31, 1994 (hereinafter "Chen"). In particular, the Examiner states that, regarding claims 22 and 32, neither the allegedly admitted prior art nor Chiang teaches an interconnect wherein a spacer is disposed on the vertical portion of the low-k material in the vias between the low-k dielectric and the conductive feature. However, the Examiner further states that Chen teaches an interconnect wherein a spacer (28) is disposed on the vertical portion of the dielectric. The Examiner states that it would have been obvious to one of ordinary skill at the time of the invention to incorporate the teaching of Chen into Chiang's device since the sidewall spacer will prevent lateral diffusion of impurities. Regarding claim 33, the Examiner states that neither the allegedly admitted prior art nor

Chiang or Chen teach an interconnect structure including a liner over a spacer. However, the Examiner further contends that it is conventional in the art to employ liners in interconnect structures, and it would have been obvious to one of ordinary skill to do so, since it is desirable to prevent impurities from diffusing to unwanted areas of the device. Applicants respectfully traverse this rejection.

Applicants assert that, even if the proposed combination were made, Applicants' claimed invention would not be obtained. Specifically, neither the allegedly admitted prior art nor Chiang, nor Chen, either alone or in combination, discloses, teaches, or suggests all of the elements recited in Applicants' claims 22, 32, and 33. In particular, with respect to claim 22, which depends from independent claim 16, Applicants assert that, for the reasons set forth above, none of the references cited by the Examiner discloses, teaches, or suggests a protective layer which covers at least one vertical portion of a low-k material. Consequently, Applicants assert that neither the allegedly admitted prior art, nor Chiang, nor Chen discloses, teaches, or suggests all of the elements of Applicants' claimed invention.

Moreover, regarding claims 32 and 33, which each depend from independent claim 28, Applicants assert that, for the reasons set forth above, none of the cited references discloses, teaches, or suggests "a second dielectric material formed above said metal lines"; "a protective layer interposed between said low-k dielectric structures and said second dielectric material"; and "a conductive feature formed within said second dielectric material and said protective layer".

For, *inter alia*, the above reasons, Applicants assert that claims 22, 32, and 33 are not rendered obvious by the allegedly admitted prior art and Chiang in view of Chen. Accordingly, claim 22, 32, and 33 are patentable over the references cited by the Examiner, and Applicants respectfully request the withdrawal of the rejection of claims 22, 32, and 33 under 35 U.S.C. §103(a).

In addition to the above reasons, dependent claim 33 is not obvious over allegedly admitted prior art and Chiang in view of Chen for independent reasons. In

particular, claim 33 further recites "a spacer interposed between said low-k material and a liner". The Examiner contends that Chen teaches an interconnect wherein a spacer (28) is disposed on the vertical portion of the dielectric. The Examiner further contends that it would have been obvious to incorporate the teaching of Chen into Chiang's device since the sidewall spacer will prevent lateral diffusion of impurities. With respect to claim 33, the Examiner then contends that, while neither Chiang nor Chen teaches a liner over a spacer, it would have been obvious to incorporate a liner since it is desirable to prevent impurities from diffusing to other areas of the device. Respectfully, Applicants disagree. Applicants assert that none of the references discloses, teaches, or suggests the desirability of "a spacer interposed between said low-k material and a liner". Even if, *arguendo*, Applicants' liner prevents lateral diffusion of impurities, none of the references cited by the Examiner suggests the desirability of a liner disposed above a spacer, especially if, *arguendo*, the spacer could also prevent lateral diffusion of impurities, as the Examiner contends. Applicant respectfully submits that there is no suggestion or motivation, either in the references cited by the Examiner or in the knowledge generally available to one of ordinary skill in the art, to provide an interconnect structure having "a spacer interposed between said low-k material and a liner". Consequently, Applicants' claim 33 is not obvious over the allegedly admitted prior art and Chiang in view of Chen. Accordingly, claim 33 is independently allowable under 35 U.S.C. §103(a).

Havemann

Claims 21, 24-26, 30, and 31 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Havemann. In particular, regarding claim 21, the Examiner states that even though Havemann does not teach a protective layer comprising silicon carbon, it would have been obvious to one of ordinary skill in the art to use silicon carbon, since it is a known material that is suited for the intended use. Regarding claim 24, the Examiner states that even though Havemann does not teach a metal filling made of tungsten and a second metal layer made of an aluminum alloy, it would have been obvious to one of ordinary skill in the art to select tungsten, since it is well known

to use tungsten plugs in interconnect devices, and it would have been obvious to use an aluminum alloy for the second metal layer, since it is a known material that is suited for the intended use. Regarding claim 25, the Examiner states even though Havemann does not teach the use of aluminum alloy for the metal filling and the second metal layer, it would have been obvious to one of ordinary skill in the art to use an aluminum alloy, since it is a known material that is suited for the intended use. Regarding claim 26, the Examiner states that even though Havemann does not teach a low-k material comprising an organic low-k material, it would have been obvious to one of ordinary skill in the art to use an organic low-k material, since it is a known material that is well suited for the intended use. Regarding claims 30 and 31, the Examiner states that even though Havemann does not teach an interconnect including a liner, it is conventional in the art to include liners in interconnect devices and would have been obvious to one of ordinary skill in the art to incorporate a liner to prevent unwanted diffusion of impurities. Applicants respectfully traverse this rejection.

Applicants respectfully submit that the prior art reference cited by the Examiner does not render the claimed invention obvious. Applicants assert that, even if the proposed modifications were made, Applicants' claimed invention would not be obtained. Specifically, for the reasons set forth above in traverse of the rejection under 35 U.S.C. §102, Havemann (the single reference cited by the Examiner) does not disclose, teach, or suggest a number of the elements in claims 21, 24-26, 30, and 31. In particular, with respect to claims 21 and 24-26, Applicants assert that Havemann does not disclose, teach, or suggest a protective layer which covers at least one vertical portion of a low-k material. Moreover, regarding claims 30 and 31, Applicants assert that Havemann does not disclose, teach, or suggest a protective layer configured to provide etch selectivity between the protective layer and the second dielectric material. Accordingly, Applicants assert that the Havemann reference does not disclose, teach, or suggest all of the elements of Applicants' claimed invention.

For, *inter alia*, the above reasons, Applicants assert that claims 21, 24-26, 30, and 31 are not rendered obvious by Havemann. Accordingly, claims 21, 24-26, 30, and

31 are patentable over Havemann, and Applicants therefore respectfully request the withdrawal of the rejection of claims 21, 24-26, 30, and 31 under 35 U.S.C. §103(a).

Havemann and Chen

Claims 22, 32, and 33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Havemann as applied to claims 16-21 and 23-31 in view of Chen. In particular, the Examiner states that, regarding claims 22 and 32, Havemann does not teach a spacer between the low-k dielectric and the conductive material. However, the Examiner contends that Chen teaches an interconnect wherein a spacer is disposed on the vertical portion of the dielectric, and it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Chen into Havemann's device, since the sidewall spacer will prevent lateral diffusion of impurities. Regarding claim 33, the Examiner states that neither Havemann nor Chen teach an interconnect structure comprising a liner between the spacer and the conductive material. However, the Examiner contends that it would have been obvious to one of ordinary skill in the art to incorporate a liner, since it is desirable to prevent unwanted diffusion of impurities.

As a preliminary matter, Applicants assert that, even if the proposed combination were made, Applicants' claimed invention would not be obtained. Specifically, none of the references cited by the Examiner, either alone or in combination, discloses, teaches, or suggests all of the elements recited in Applicants' claims 22, 32, and 33. For the reasons set forth above in traverse of the rejections under 35 U.S.C. §102 and 35 U.S.C. §103 in view of Havemann alone, Applicants assert that Havemann (the primary reference cited by the Examiner) does not disclose, teach, or suggest a number of the elements in claims 22, 32, and 33. In particular, with respect to claim 22, Applicants assert that Havemann does not disclose, teach, or suggest a protective layer which "covers at least one vertical portion of the low-k material". Moreover, regarding claims 32 and 33, Applicants assert that Havemann does not disclose, teach, or suggest a protective layer "configured to provide etch selectivity between the protective layer and the second dielectric material". Accordingly, Applicants assert that the Havemann

reference does not disclose, teach, or suggest all of the elements of Applicants' claimed invention.

Additionally, Chen (the secondary reference cited by the Examiner) also does not disclose, teach, or suggest all of the elements recited in Applicants' claims 22, 32, and 33. Specifically, Chen does not disclose, teach, or suggest a protective layer which covers at least one vertical portion of a low-k material, as recited in Applicants' independent claim 16, the claim from which claim 22 depends. Moreover, Chen does not disclose, teach, or suggest a protective layer configured to provide etch selectivity between the protective layer and the second dielectric material, as recited in Applicants' independent claim 28, the claim from which claims 32 and 33 each depend.

For, *inter alia*, the above reasons, Applicants assert that claims 22, 32, and 33 are not rendered obvious by Havemann in view of Chen. Accordingly, claim 22, 32, and 33 are patentable over the references cited by the Examiner, and Applicants therefore respectfully request the withdrawal of the rejection of claims 22, 32, and 33 under 35 U.S.C. §103(a).

In addition to the above reasons, dependent claim 33 is not obvious over Havemann in view of Chen for independent reasons. In particular, claim 33 further recites "a spacer interposed between said low-k material and a liner". The Examiner contends that Chen teaches an interconnect wherein a spacer (28) is disposed on the vertical portion of the dielectric. The Examiner further contends that it would have been obvious to incorporate the teaching of Chen into Havemann's device since the sidewall spacer will prevent lateral diffusion of impurities. With respect to claim 33, the Examiner then contends that, while neither Havemann nor Chen teaches a liner between the spacer and the conductive material, it would have been obvious to incorporate a liner since it is desirable to prevent unwanted diffusion of impurities. Applicants respectfully disagree. Applicants assert that none of the references discloses, teaches, or suggests the desirability of "a spacer interposed between said low-k material and a liner". Even if, *arguendo*, Applicant's liner prevents lateral diffusion of impurities, none of the references cited by the Examiner suggests the desirability of a liner disposed above a

spacer, especially if, *arguendo*, the spacer could also prevent lateral diffusion of impurities, as the Examiner contends. Applicant respectfully submits that there is no suggestion or motivation, either in the references cited by the Examiner or in the knowledge generally available to one of ordinary skill in the art, to provide an interconnect structure having "a spacer interposed between said low-k material and a liner". Consequently, Applicants' claim 33 is not obvious over Havemann in view of Chen. Accordingly, claim 33 is independently allowable under 35 U.S.C. §103(a).

CONCLUSION

In view of the foregoing, Applicants respectfully submit that all of the pending claims fully comply with 35 U.S.C. §112 and are allowable over the prior art of record. No new matter is added by this Amendment. Reconsideration of the application and allowance of all pending claims is earnestly solicited. Should the Examiner wish to discuss any of the above in greater detail or deem that further amendments should be made to improve the form of the claims, then the Examiner is invited to telephone the undersigned at the Examiner's convenience.

Dated: September 28, 2000

Respectfully submitted,

By: _____
Randee S. Schwartz
Reg. No. 45,085

Pillote, Cindy
602-382-6296

SNELL & WILMER L.L.P.
One Arizona Center
400 East Van Buren
Phoenix, Arizona 85004-2202
Telephone: (602) 382-6332
Facsimile: (602) 382-6070